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| EXAMINER | |
|---|---|
| MEONSKE, TONIA L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/870,458 | CONNER ET AL. | |
| | Examiner | Art Unit | |
| | Tonia L. Meonske | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/14/06 (11 pages)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS filed 2/6/06 (11 pages)*.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 15, 2006 has been entered.

### *Information Disclosure Statement*

2. The information disclosure statement filed August 14, 2006 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. The Japanese patent citation "P" been placed in the application file, but the information referred to therein has not been considered as a complete legible copy has not been provided.

3. The 11 page IDS filed February 6, 2006 is a duplicate copy of the 11 page IDS filed on August 14, 2006. The IDS filed February 6, 2006 is not considered because it is a duplicate copy of an already considered IDS.

### *Claim Objections*

4. Claim 20 is objected to because of the following informalities: Claim 20, lines 1-2 contains the following redundant limitation "where the second shift operation is a multi-precision shift instruction." This limitation initially appears in claim 19, line 9. The

redundant information should be deleted from claim 20. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 19-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 19 recites the limitation "the first shift instruction and second shift instruction" in line 10. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination "the first shift instruction and second shift instruction" will be interpreted as "the first shift operation and second shift operation". Claims 20-28 are dependent on 19, either directly or indirectly, and are therefore rejected for incorporating the defects of claim 19. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 19-26 and 28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3:

Architecture and Programming Manual, pages 3-2, 18-7, 25-289 to 25-292, which were cited by Examiner on March 25, 2004 and pages 4-13 to 4-17, which are cited herein (herein after "Intel").

10. Referring to claim 19, Intel has taught a method, implemented in a computer system, of shifting a multi-word value comprising:

a. performing a first shift operation on a first portion of the multi-word value to produce one or more overflow bits (Pages 4-16 and 4-17, pages 25-289 to 25-292, Bits are shifted out of the source register.);

b. performing a second shift operation on a second portion of the multi-word value (Pages 4-16 and 4-17, pages 25-289 to 25-292, Bits are shifted in the destination register.),

c. where the second shift operation comprises:

i. producing a shift result; and concatenating the shift result and the overflow bits (Pages 4-16 and 4-17, pages 25-289 to 25-292, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.) and

ii. where the second shift operation is a multi-precision shift instruction (pages 25-289 to 25-292, SHRD and SHLD are double (or multi) precision shift right/left instructions. The second shift operation shifts by 64 bits or more, therefore the second shift operation is a multi-precision shift instruction.) and where the first shift instruction and second shift instruction are performed sequentially (The first operation produces

overflow bits. The second operation concatenates a shift result with the overflow bits produced from the first operation. Therefore, the second operation must be sequential to the first operation since the second operation cannot be performed until the first operation has completed and produced the overflow bits.).

11. Referring to claim 20, Intel has taught the method of claim 19, where the second shift operation is a multi-precision shift instruction (pages 25-289 to 25-292, SHRD and SHLD are double (or multi) precision shift right/left instructions. The second shift operation shifts by 64 bits or more, therefore the second shift operation is a multi-precision shift instruction.), and where the second shift operation produces a result (Pages 4-16 and 4-17, A result is stored back into, or output to the destination operand.), the method further comprising:

a. fetching and decoding the multi-precision shift instruction (Page 18-7, First paragraph, Instructions are inherently fetched and decoded in the processing system in order for to be executed, Pages 4-16 and 4-17, pages 25-289 to 25-292, SHLD and SHRD are multi-precision shift instructions.); and

b. outputting the result (Pages 4-16 and 4-17, pages 25-289 to 25-292, The result is stored back into, or output to the destination operand.).

12. Referring to claim 21, Intel has taught the method of claim 20, as described above, and where the multi-precision shift instruction is a shift left instruction (Page 4-16, 25-289 and 25-290, SHLD).

13. Referring to claim 22, Intel has taught the method of claim 20, as described above, and where the multi-precision shift instruction is a shift right instruction (Pages 4-16, 4-17, 25-291 and 25-292, SHRD).

14. Referring to claim 23, Intel has taught the method of claim 20, as described above, and where the multi-precision shift instruction specifies a shift increment (Pages 4-16 and 4-17, The CL register or an immediate byte in the instruction specifies the number of bits to be shifted.).

15. Referring to claim 24, Intel has taught the method of claim 20, as described above, and where the shift increment is greater than or equal to the number of bits in a word (Page 4-16 and 4-17, pages 25-289 to 25-292, When the shift increment is greater than or equal to the number of bits in a 32-bit word then the increment is taken modulo 32.).

16. Referring to claim 25, Intel has taught the method according to claim 20, as described above, and where the shift increment is less than the number of bits in a word (Pages 4-16, 25-289 to 25-290, The shift increment is 0 to 31 bits and a word is 32 bits.).

17. Referring to claim 26, Intel has taught the method of claim 19, as described above, and further comprising:

a. storing one or more bits shifted out of the second portion of the multi-word value during the second shift instruction in a carry register (Pages 4-16 and 4-17, Bits shifted out of the destination register are stored in CF.).

18. Referring to claim 28, Intel has taught the method of claim 19, as described above, and further comprising:

a. storing one or more of the overflow bits in a carry register (Pages 4-16 and 4-17, Overflow bits from the source are stored in the destination register.).

***Claim Rejections - 35 USC § 103***

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 27 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual, pages 3-2, 18-7, 25-289 to 25-292, which were cited by Examiner on March 25, 2004 and pages 4-13 to 4-17, which are cited herein (hereinafter "Intel"), in view of Silverbrook, US Patent 6,314,200, cited by Examiner on March 25, 2004 (Herein after "Silverbrook").

21. Referring to claim 27, Intel has taught the method of claim 19, as described above. Intel has not specifically taught all of the logical operations required to implement the shift instructions. Specifically, Intel has not taught where concatenating the shift result and the overflow bits comprises: performing a logical OR operation on at least one bit in the shift result and at least one overflow bit. However, Silverbrook et al. have taught performing a logical OR operation on at

least one bit in a shift result and at least one overflow bit (column 222, lines 10- 24) in order to easily implement multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Intel, include performing the claimed OR operation, as taught by Silverbrook et al., for the desirable purpose of easily implementing multiple precision shifting (column 222, lines 10-24).

22. Referring to claim 29, Intel has taught a processor for processing multi-precision shift instructions, comprising:

a. a program memory for storing instructions including at least one multi-precision shift instruction (Page 3-2, lines 1-3, The program code, or instructions, are stored in the memory. SHLD and SHRD instructions are multi-precision shift instructions, see 4-16, 4-17 and 25-289 to 25-292.);

b. a program counter for identifying current instructions for processing (Page 3-15, section 3.3.5, Instruction Pointer), and

c. a shifter for executing shift instructions, including the at least one multi-precision shift instruction (Pages 4-16 and 4-17, SHLD and SHRD), the shifter including:

i. one or more carry registers for storing values shifted out of sections of the shifter (Page 4-16 and 4-17, CF); and

ii. logic for concatenating values stored in one or more carry registers with values in the shifter (Page 4-16 and 4-17, pages 25-289

to 25-292, A lower portion of bits of the destination are concatenated with the bits shifted out of the source register.); and

d. where the shifter is operable to shift a multi-word value (Pages 4-16 and 4-17, SHLD and SHRD shift doubleword (or multi-word) operands.), and where when shifting a multi-word value the shifter:

i. executes at least one shift instruction to:

(1) load a first operand into a section within the shifter, where the first operand is a first portion of the multi-word value (Pages 4-16 and 4-17, The source operand is loaded into the source register.); and

(2) generate one or more overflow bits (Pages 4-16 and 4-17, Bits are shifted out of the source register.); and

ii. executes at least one multi-precision shift instruction fetched from the program memory (Pages 4-16 and 4-17, The SHRD and SHLD instruction are executed.) to:

(1) load a second operand into a section within the shifter, where the second operand is a second portion of the multi-word value (Pages 4-16 and 4-17, The destination operand is loaded into the destination register.);

(2) shift the operand; concatenate the operand with one or more of the overflow bits (Pages 4-16 and 4-17, A lower portion of bits

of the destination are concatenated with the bits shifted out of the source register.); and

(3) output the shifted value (Pages 4-16 and 4-17, The result is stored back into, or output to the destination operand.).

23. Intel has omitted hardware details of the shifter. Intel has not taught specifically that the shifter is a barrel shifter. However, barrel shifters are known to shift a word a certain number of bits in either direction in a single clock cycle. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the shifter of Intel be a barrel shifter so that the shift instructions, which shift words a certain number of bits in either direction, would have been executed in a single clock cycle. Official Notice has been taken.

24. Intel has not specifically taught all of the logic required to implement the shift instructions. Intel has not specifically taught OR logic for concatenating values stored in the one or more carry registers with values in the shifter. Silverbrook et al. have taught OR logic for concatenating values stored in carry registers with values in a shifter (column 222, lines 10-24) in order to easily implement multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Intel, include the claimed OR logic, as taught by Silverbrook et al., for the desirable purpose of easily implementing multiple precision shifting (column 222, lines 10-24).

25. Claims 30, 31 and 34 do not recite limitations above the claimed invention set forth in claims 21, 22 and 23, respectively and are therefore rejected for the same reasons set forth in the rejection of claims 21, 22 and 23 above.

26. Referring to claim 32, Intel has taught the processor of claim 29, as described above, and where the multi-precision shift instruction is an arithmetic shift instruction (Pages 4-13 to 4-17, SHLD is equivalent to an arithmetic instruction.).

27. Referring to claim 33, Intel has taught the processor of claim 29, as described above, and where the multi-precision shift instruction is a logical shift instruction (Pages 4-13 to 4-17, SHLD is a logical shift instruction.).

***Response to Arguments***

28. Applicant's arguments filed August 14, 2006 have been fully considered but they are not persuasive.

29. On page 6 of the remarks, Applicant argues in essence:

> *"Applicants have amended claim 19 to show that the first and second shift operations are separate sequential shift operations, unlike the double-shift instructions of Intel. Applicants therefore request reconsideration of claims 19-28."*

However, claim 19 has specifically been amended to include "where the second shift operation is a multi-precision shift instruction and where the first shift instruction and second shift instruction are performed sequentially". Intel has in fact taught where the second shift operation is a multi-precision shift instruction *(pages 25-289 to 25-292, SHRD and SHLD are double (or multi) precision shift right/left instructions. The second shift operation shifts by 64 bits or more,*

*therefore the second shift operation is a multi-precision shift instruction.)* and where the first shift instruction and second shift instruction are performed sequentially *(The first operation produces overflow bits. The second operation concatenates a shift result with the overflow bits produced from the first operation. Therefore, the second operation must be sequential to the first operation since the second operation cannot be performed until the first operation has completed and produced the overflow bits.).* Also see the rejection of claim 19 above. Therefore this argument is moot.

***30.*** Applicant's arguments with respect to claims 29-34 have been considered but are moot in view of the new ground(s) of rejection above.

***Conclusion***

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

Tonia L. Meonske 10/24/2006

Tonia L. Meonske